Session 22 Overview

Low Power Multimedia

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Multimedia processing is becoming a critical requirement and a major driver of present day and future consumer electronics equipment such as game consoles, mobile handsets, home entertainment systems, etc. With the availability of increasing data bandwidth, there is a greater demand for much more advanced multimedia processing capabilities, which in turn translates to higher computational and storage requirements on these devices. Compounding this challenge is the ever increasing demand for mobility, dictating that these multimedia functions be performed at the lowest levels of power consumption.

The seven papers in this session focus on recent advances in low power multimedia processing integrated circuits that deliver advanced functionality, such as 3D graphics, high resolution still and video encoding/decoding, and high fidelity audio playback. Results from these papers demonstrate that smart architecture design and implementation techniques, in conjunction with advanced process technology, can deliver very high performance multimedia functionalities at very low power consumption levels.

A 0.18µm CMOS MPEG-2/H.264 video decoder is described in Paper 22.1. The decoder, which employs a scalable pipeline and a prediction circuit to reduce memory bandwidth, performs real-time MPEG-2 and H.264/AVC decoding at 108µW and 125µW, respectively. Paper 22.2 describes a 345mW JPEG 2000 codec in 0.18µm CMOS, capable of achieving a throughput of 124MSamples/s to support high definition (1920×1080) video encoding and decoding. In their paper, the authors discuss a scheduling scheme that reduces 192KB tile memory and techniques to reduce silicon area by 40%. Paper 22.3 describes a H.264 video decoder in 0.18µm CMOS that operates at 120MHz for high definition video (HD1080, 1920×1088@30Hz) while dissipating 320mW. The internal memory size and gate-count have also been reduced through appropriate algorithmic and architectural changes.

Multimedia processor chips are described in the next two papers. Paper 22.4 describes a VLIW graphic processor that achieves up to 120Mvertices/sec of 3D geometry. The processor supports OpenGL ES 2.0 and Vertex Shader model 3.0 while consuming approximately 50% of the energy of a conventional SIMD implementation. Paper 22.5 presents a massively parallel SIMD processor based on the Matrix architecture that achieves 40GOPS (16b additions) at 200MHz while dissipating 250mW. The processor occupies 3.1mm^2 in 90nm CMOS, and is targeted for consumer-based computer vision and video recognition applications.

Paper 22.6 presents a 5mW MPEG4 Simple Profile encoder in 0.18µm CMOS technology that encodes CIF 30fps in real-time at 9.5MHz. Power reduction is achieved by a 2-D bandwidth-sharing ME design, content-aware DCT/IDCT algorithm, and clock gating techniques Paper 22.7 presents a multimedia processor that achieves 6.33mW decoding for MPEG audio in 0.15µm CMOS at 1.1V supply. To reduce power consumption, parallel processing DSP and conditional pre-charge sense-amp based flip-flop are used.

22.1 **A 125µW Fully Scalable MPEG-2 and H.264/AVC Video Decoder for Mobile Applications** **8:30 AM**
T-M. Liu, National Chiao Tung University, Hsinchu, Taiwan

An MPEG-2 and H.264/AVC decoder occupies 3.9×3.9mm² in 0.18µm 1P6M CMOS. To improve integration efficiency and transmission bandwidth, a scalable pipeline and prediction circuit is employed. The decoder performs real-time MPEG-2 and H.264/AVC QCIF at 15frames/s video decoding, dissipating 108µW and 125µW, respectively, at 1V with a clock frequency of 1.15MHz.

22.2 **124MS/s Pixel-Pipelined Motion-JPEG 2000 Codec without Tile Memory** **9:00 AM**
Y-W. Chang, National Taiwan University, Taipei, Taiwan

A JPEG2000 codec capable of processing 1920×1080 HD video at 30frames/s is implemented on a 20.1mm² die with 0.18µm CMOS technology dissipating 345mW at 1.8V and 42MHz. The level-switched schedule eliminates the 192kB tile memory. Hardware sharing between encoder and decoder reduces silicon area by 40%.

22.3 **A 160kGate 4.5kB SRAM H.264 Video Decoder for HDTV Applications** **9:30 AM**
C-C. Lin, National Chung Cheng University, Chia-Yi, Taiwan

Through both algorithmic and architectural optimization, the H.264 video decoder dissipates 320mW at 1.8V when operating at 120MHz for HD1080 (1920×1088 at 30frames/s). The die contains 160kgates 4.5kB memory and occupies 2.9×2.9mm² in 0.18µm CMOS.

22.4 **A 120Mvertices/s Multi-Threaded VLIW Vertex Processor for Mobile Multimedia Applications** **10:15 AM**
C-H. Yu, KAIST, Daejeon, Korea

A 3D vertex processor with a floating-point 4-threaded and 4-issue VLIW architecture and a TnL vertex cache is implemented for mobile multimedia applications in a 0.18µm 4M CMOS process. The proposed architecture efficiently reduces the total energy consumption and achieves 120Mvertices/s with a 2.5GFLOPS datapath using 157mW when operating at 100MHz.

22.5 **A 40GOPS 250mW Massively Parallel Processor Based on Matrix Architecture** **10:45 AM**
M. Nakajima, Renesas Technology, Itami, Japan

The Matrix Processing Engine (MTX) is a massively parallel processor based on the Matrix architecture. 40GOPS (16b additions) is achieved at 200MHz clock frequency and 250mW power dissipation. 2048 ALUs and 1Mb SRAM connected by a flexible switching network are integrated in 3.1mm² using a 90nm CMOS process.

22.6 **A 5mW MPEG4 SP Encoder with 2D Bandwidth-Sharing Motion Estimation for Mobile Applications** **11:15 AM**
C-P. Lin, National Taiwan University, Taipei, Taiwan

A 5mW MPEG4 SP encoder is implemented on a 7.7mm² die in 0.18µm CMOS technology. It encodes CIF 30frames/s in real-time at 9.5MHz using 5mW at 1.3V and VGA 30frames/s at 28.5MHz uses 18mW at 1.4V. This chip employs a 2D bandwidth-sharing ME design, content-aware DCT/IDCT, and clock gating techniques to minimize power consumption.

22.7 **6.33mW MPEG Audio Decoding on a Multimedia Processor** **11:45 AM**
Y. Ueda, SANYO Electric, Gifu, Japan

Low-power implementation techniques are used in the multimedia processor to achieve MPEG audio decoding in 6.33mW with a 1.1V supply. Three techniques are employed: a parallel processing DSP; dynamic voltage control using a multi-power domain; and a conditional pre-charge flip-flop. The processor occupies 6.5×6.5mm² in 0.15µm 6M CMOS.